Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
Li.	2033386	divid\$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/03 13:10
L2	999285	clock\$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/03 13:10
L3	260783	1 and 2	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/03 13:12
L4	96158	limit\$4 SAME amplitude	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/03 13:12
L5	11082	3 and 4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/03 13:13
L6	585	delay adj matching	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/03 13:13
L7	19	5 and 6	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/03 13:13
L8	103796	steady adj state	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/03 13:14

L9	8	7 and 8	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/03 13:17
L10	4315	clock adj buffer\$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/03 13:18
L11	8338	divid\$4 adj clock\$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/03 13:19
L12	277	10 and 11	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/03 13:19
L13	14	12 and 4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/03 13:19
L14	9	13 not 9	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/03 13:20
L15	15729	amplitude near1 adjust\$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/03 13:21
L16	7	15 and 12	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/03 13:23

L17	14	12 and 4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/03 13:24
L18	1362	limit\$4 SAME amplitude SAME (steady adj state)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/03 13:25
L19	617	18 and 1	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/03 13:29
L20	150	19 and 2	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/03 13:28
L21	0	out adj of adj phase	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/03 13:28
L22	7786582	(out of phase)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/03 13:29
L23	276	2 and 18	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/03 13:29



Fax \boxtimes	Urgent 🗌 Retu	urn reply requested Original will be sent as confirmation
To: USPTO		Date: March 3, 2005
Attention: Examiner	M. Ton	Re: Appl. No. 10/622,708; Filed 07/21/03 For: Apparatus and Method for Delay Matching of Full and Divided Clock
From: Jason D. Eiser	iberg	Signals Inventor: Kwang Y. Kim
Pages (including cove	er sheet): 5	Your Reference: 10/622,708
Fax No: (571) 273-17	754	Our Reference: 1875.1710002

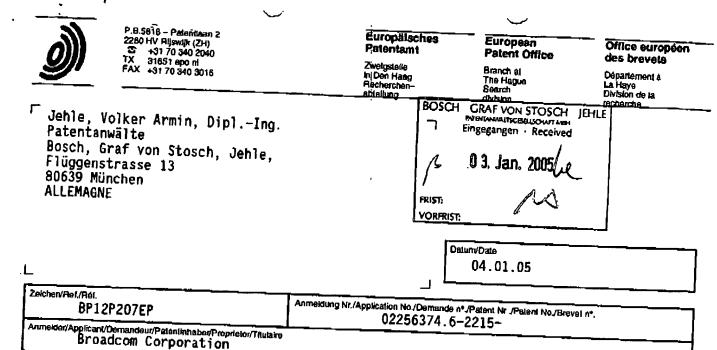
Message

The European Search Report and Japanese Abstract filed on January 19, 2005 are attached.

If any portion of this transmission is not received clearly or in full, contact us at 202.371.2600 or f 202.371.2540

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COMMUNICATION

The European Patent Office herewith transmits as an enclosure the European search report for the above-mentioned European patent application,

If applicable, copies of the documents cited in the European search report are attached.

Additional set(s) of copies of the documents cited in the European search report is (are) enclosed

The following specifications given by the applicant have been approved by the Search Division:

Abstract

⚠ tille

The abstract was modified by the Search Division and the definitive text is attached to this

The following figure will be published together with the abstract:

3

REFUND OF THE SEARCH FEE

If applicable under Article 10 Rules relating to fees, a separate communication from the Receiving Section on the refund of the search fee will be sent later.



EPO FORM 1503 03.82 (PO4COL)



EUROPEAN SEARCH REPORT

Application Number

EP 02 25 6374

	CONSTITUTE CONS	SIDERED TO BE RELEVAN	т	7
Category	Of relevant	ilth Indication, where appropriate, passages	Relevant to claim	CLASSIFICATION OF THE
	US 5 175 752 A () 29 December 1992 * f1gure 3 *	OKOMIZO KOICHI) (1992-12-29)		HO3K5/13
8 C	PATENT ABSTRACTS /01. 0131, no. 73 24 April 1989 (19 3 JP 64 002417 A CORP), 6 January 3 abstract; figure	(E-748), 89-04-24) (MITSUBISHI ELECTRIC	1,4	
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				TECHNICAL FIELDS SEARCHED (Int.CL7)
				103К
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The p	present search report has be	en drawn up for all claims	1	Ĭ
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CATEGOR Particularly in particularly in locument of echnological	RY OF CITED DOCUMENTS clevant if taken alone elevant if combined with another the same category i background disclosure	L: document cled in t	neni, but published o	on n, or

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO.

EP 02 25 6374

This annex tiles the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP, file on The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

04

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	US 5175752	A	29-12-1992	JP	4151912 A	25-05-1992
	JP 64002417	A	06-01-1989	NONE		50-03-1997
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EUROPEAN PATENT OFFICE

Patent Abstracts of Japan

PUBLICATION NUMBER

64002417

PUBLICATION DATE

06-01-89

APPLICATION DATE

24-06-87

APPLICATION NUMBER

62158279

APPLICANT: MITSUBISHI ELECTRIC CORP;

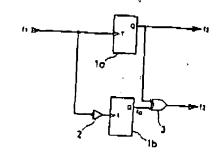
INVENTOR: YAMASHITA SHINJI;

INT.CL.

: H03K 23/50

TITLE

: FREQUENCY DIVIDER



ABSTRACT: PURPOSE: To preclude the skew between a signal after frequency division and an original signal by generating 1/2-frequency-divided signals by a frequency dividing circuit at each timing which is 0 and $\pi/2$ each out of phase with the input signal, ORing the two frequency divided signals which differ in timing exclusively, and regenerating a signal similar to the frequency of the input signal.

> CONSTITUTION: This frequency divider consists of 1st and 2nd frequency dividing circuits 1a and 1b which output frequency signals a half as large as the input signal, an inverter circuit 2 which outputs the inverted signal of the input signal, and a two-input exclusive OR circuit 3. The exclusive OR output signal f_2 between the output signal f_3 of the frequency dividing circuit 1a which inputs the input signal f_1 and the output signal f_2 of the frequency dividing circuit 1b which inputs the output of the inverter circuit 2 for the input signal f_1 is generated to generate the signal f_2 similar to the frequency of the original input signal f₁. The signal delay propagation of the exclusive OR circuit is smaller than that of an FF circuit, so this regenerated signal f_2 is used instead of the original input signal f₁. Consequently, the skew between the original frequency signal and 1/2 frequency

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